10. The microprocessor as recited in claim 1 wherein the control register comprises:

an interrupt mask bit field, said interrupt mask bit field having a plurality of bits, each of said plurality of bits for identifying interrupts received by the microprocessor.

11. The microprocessor as recited in claim 10 wherein by atomically clearing one of said plurality of bits using the privileged instruction, its corresponding interrupt is temporarily disabled.

12. A method for atomically modifying interrupt mask bits within a privileged control register of a microprocessor, the method comprising:

providing a privileged instruction which instructs the microprocessor to clear particular ones of the interrupt mask bits;

providing a bit mask, for specifying which of the particular ones of the interrupt mask bits are to be cleared; and

upon receipt of an interrupt by the microprocessor, atomically clearing the particular ones of the interrupt mask bits as specified by the bit mask.

13. The method as recited in claim 12 wherein the interrupt mask bits specify which of a plurality of interrupts have been received by the microprocessor.

14. The method as recited in claim 12 wherein the interrupt mask bits specify which of a plurality of interrupts are enabled.

15. The method as recited in claim 12 wherein the privileged control register comprises a status register having a plurality of bit fields, including the interrupt mask bits.

16. The method as recited in claim 12 wherein the privileged instruction comprises:

an opcode for designating the privileged instruction as privileged;

a first operand for designating the privileged control register as the register to be modified; and

a second operand for designating the location of the bit mask.

17. The method as recited in claim 12 further comprising:

providing a privileged instruction which instructs the microprocessor to set particular ones of the interrupt mask bits; and

providing a bit mask, for specifying which of the particular ones of the interrupt mask bits are to be set.

18. A bit clear instruction for execution on a microprocessor having a privileged control register, the bit clear instruction executing on the microprocessor when the microprocessor receives an interrupt and when the microprocessor is in a privileged state, the bit clear instruction comprising:

a plurality of opcode bits for designating the bit clear instruction as a privileged instruction;

a plurality of first operand bits for designating the privileged control register as the register to be operated upon by the bit clear instruction; and

a plurality of second operand bits for designating a general purpose register as a register containing a bit mask, said bit mask specifying which of a plurality of bits within the privileged control register are to be cleared;

wherein when the bit clear instruction executes on the microprocessor, the plurality of bits within the privileged control register that are specified by said bit mask are cleared, atomically.

19. The bit clear instruction as recited in claim 18 wherein the privileged control register comprises a status register having an interrupt mask bit field.

20. A computer program product for use with a computing device, the computer program product comprising:

a computer usable medium, having computer readable program code embodied in said medium, for causing a microprocessor having a control register that is modifiable by a privileged instruction to be described, said computer readable program code comprising:

first program code for providing a core, for receiving the privileged instruction and for modifying the control register upon execution of the privileged instruction; and

second program code for providing the privileged instruction, the privileged instruction comprising:

an opcode, for identifying the instruction as a privileged instruction;

a first operand, for specifying the control register as a register to be modified; and

a second operand, for specifying a location of a second register within the microprocessor, said second register containing a bit mask, said bit mask determining which of the bit fields within the control register are to be modified;

wherein said bit mask is used to set or clear the bit fields in the control register;

whereby the bit fields in the control register are modified atomically by the privileged instruction.

21. The computer program product group as recited in claim 20 wherein the privileged instruction is executed when the microprocessor receives an interrupt signal.

22. The computer program product group as recited in claim 20 wherein the privileged instruction clears bit fields in the control register pertaining to corresponding bits that are set in said bit mask.

23. A computer data signal embodied in a transmission medium comprising:

computer-readable first program code for providing a bit clear instruction for execution on a microprocessor having a privileged control register, the bit clear instruction executing on the microprocessor when the microprocessor receives an interrupt and when the microprocessor is in a privileged state, said first program code comprising:

program code for providing a plurality of opcode bits for designating the bit clear instruction as a privileged instruction;

program code for providing a plurality of first operand bits for designating the privileged control register as the register to be operated upon by the bit clear instruction; and

program code for providing a plurality of second operand bits for designating a general purpose register as a register containing a bit mask, said bit mask specifying which of a plurality of bits within the privileged control register are to be cleared;

wherein when the bit clear instruction executes on the microprocessor, the plurality of bits within the privileged control register that are specified by said bit mask are cleared, atomically.